

SNA8721Q/8722Q 11MHz CMOS Rail-to-Rail IO Opamps

Features

- Single-Supply Operation from +2.1V ~ +5.5V
- Rail-to-Rail Input/Output
- Gain-Bandwidth Product: 11MHz (Typ)
- Low Input Bias Current: 1pA (Typ)
- Low Offset Voltage: 3.5mV (Max)
- High Slew Rate: 9V/μs
- Settling Time to 0.1% with 2V Step: 0.3μs
- Low Noise : 8nV/√Hz @10kHz
- Quiescent Current: 1.1mA per Amplifier (Typ)
- Operating Temperature: -40°C ~ +125°C
- Small Package:
 - SNA8721Q Available in SOT-23-5, SOP-8 and SC70-5 Packages
 - SNA8722Q Available in SOP-8, MSOP-8, TSSOP-8 and DFN2*2-8 Packages
- AEC-Q100 qualified

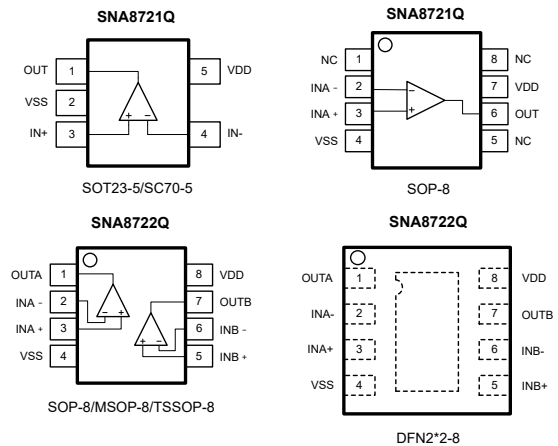
Applications

- Sensors
- Active Filters
- Cellular and Cordless Phones
- Laptops and PDAs
- Audio
- Handheld Test Equipment
- Battery-Powered Instrumentation
- A/D Converters

General Description

The SNA872X family have a high gain-bandwidth product of 11MHz, a slew rate of 9V/μs, and a quiescent current of 1.1mA per amplifier at 5V. The SNA872X are designed to provide optimal performance in low voltage and low noise systems. They provide rail-to-rail output swing into heavy loads. The input common mode voltage range includes ground, and the maximum input offset voltage is 3.5mV for SNA872X. They are specified over the extended industrial temperature range (-40°C to +125°C). The operating range is from 2.1V to 5.5V. The SNA8721Q single is available in Green SC70-5, SOT-23-5 and SOP-8 packages. The SNA8722Q single is available in Green SOP-8, MSOP-8, TSSOP-8 and DFN2*2-8 packages.

Pin Assignment



Ordering Information

Model	Channel	Package	Ordering Number	Packing Option
SNA8721Q	Single	SC70-5	SNA8721Q00CE5	Tape and Reel,3000
		SOT-23-5	SNA8721Q00CB5	Tape and Reel,3000
		SOP-8	SNA8721Q00CA8	Tape and Reel,3000
SNA8722Q	Dual	SOP-8	SNA8722Q00CA8	Tape and Reel,3000
		MSOP-8	SNA8722Q00CM8	Tape and Reel,3000
		TSSOP-8	SNA8722Q00C18	Tape and Reel,3000
		DFN2*2-8	SNA8722Q00CD8	Tape and Reel,3000

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1 Specifications

1.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power Supply Voltage (V_{DD} to V_{SS})	-0.5	+7.5	V
Analog Input Voltage (IN+ or IN-)	$V_{SS}-0.5$	$V_{DD}+0.5$	V
PDB Input Voltage	$V_{SS}-0.5$	+7	V
Operating Temperature Range	-40	+125	°C
Junction Temperature	160		°C
Storage Temperature Range	-55	150	°C
Lead Temperature (soldering, 10sec)	260		°C
Package Thermal Resistance, θ_{JA} ($T_A=+25^\circ\text{C}$)	SOP-8	125	°C/W
	MSOP-8	216	°C/W
	SOT-23-5	190	°C/W
	SC70-5	333	°C/W
ESD	HBM	8000	V
	MM	400	V

! **Attention:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

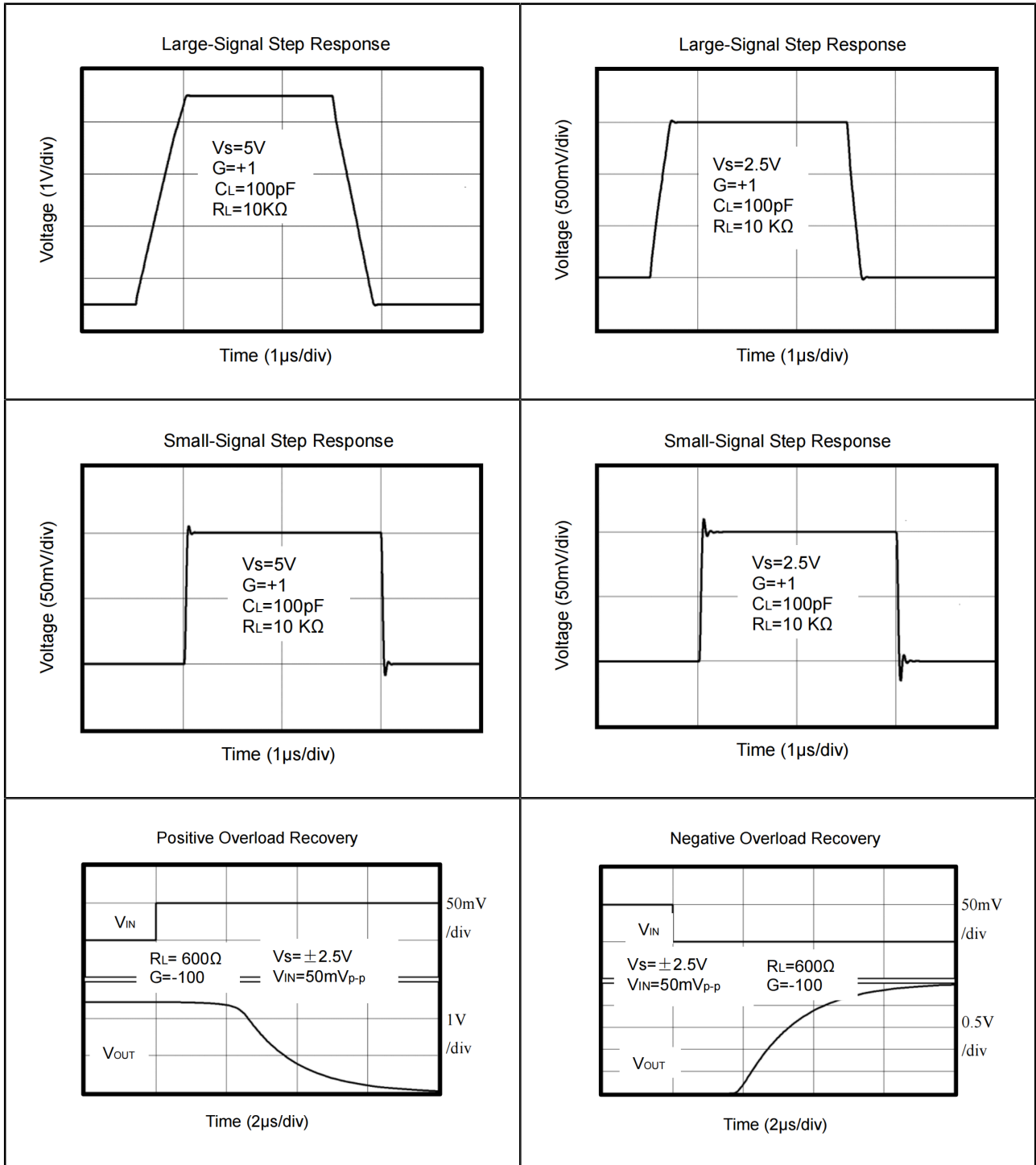
1.2 Electrical Characteristics

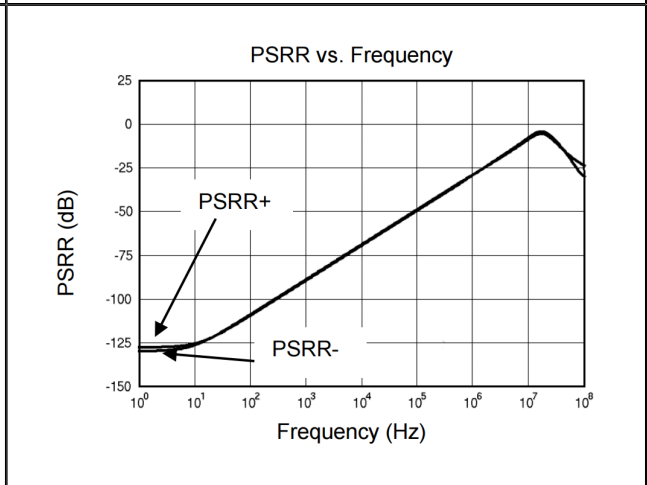
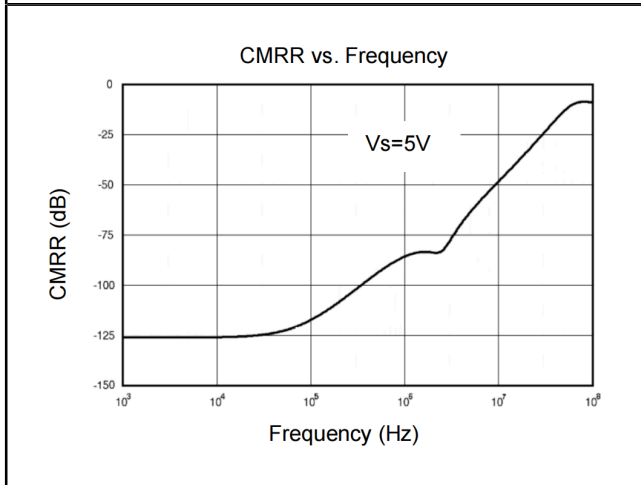
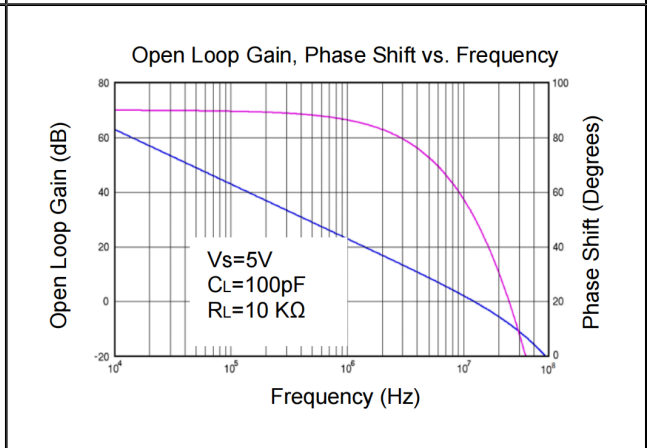
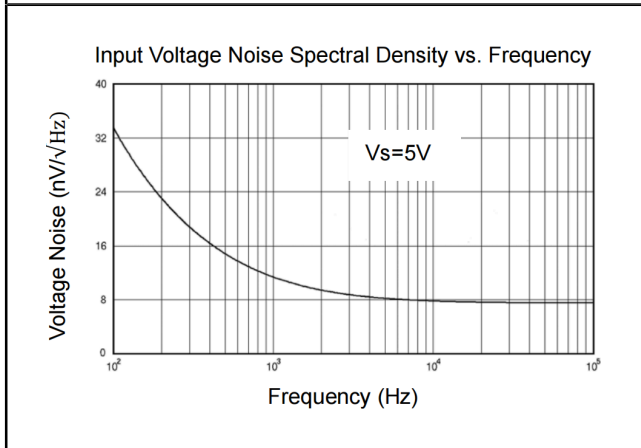
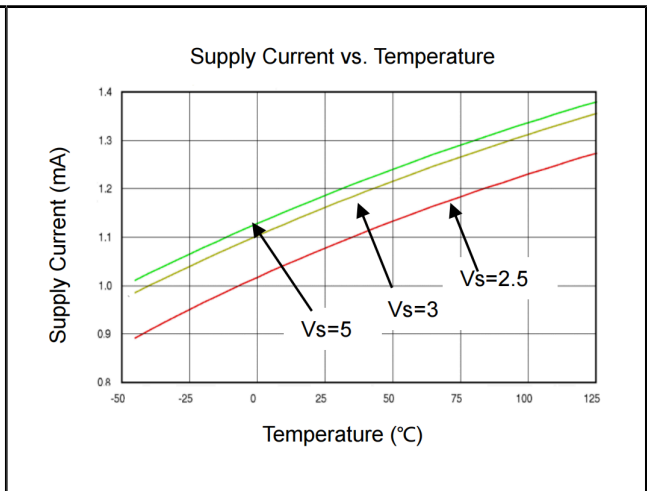
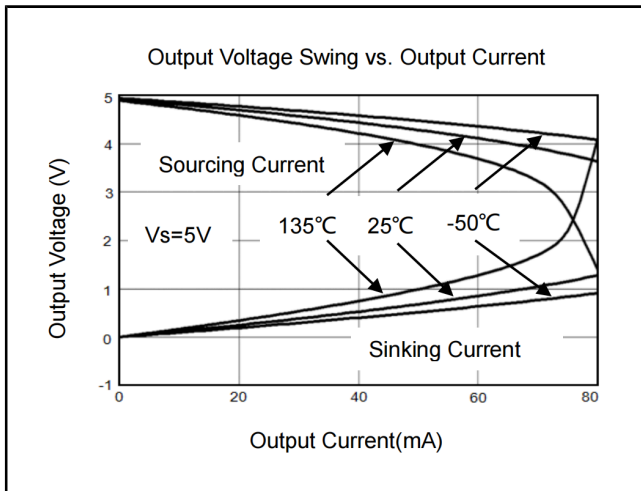
At $V_S = +5\text{V}$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L = 600\Omega$, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.8	3.5	mV
Input Bias Current	I_B			1		pA
Input Offset Current	I_{OS}			1		pA
Input Common-Mode Voltage Range	V_{CM}	$V_S = 5.5\text{V}$		-0.1~ +5.6		V
Common-Mode Rejection Ratio	CMRR	$V_S = 5.5\text{V}$, $V_{CM} = -0.1\text{V}$ to 4V	65	82		dB
		$V_S = 5.5\text{V}$, $V_{CM} = -0.1\text{V}$ to 5.6V		75		dB
Open-Loop Voltage Gain	A_{OL}	$R_L = 600\Omega$, $V_O = +0.15\text{V}$ to $+4.85\text{V}$	80	90		dB
		$R_L = 10\text{k}\Omega$, $V_O = +0.05\text{V}$ to $+4.95\text{V}$		108		dB
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.4		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing from Rail		$R_L = 600\Omega$		0.1		V
		$R_L = 10\text{k}\Omega$		0.015		V
Output Current	I_{OUT}		55	70		mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Closed-Loop Output Impedance		f = 100kHz, G = 1		7.5		Ω
POWER-DOWN DISABLE						
Turn-On Time				1.1		μs
Turn-Off Time				0.3		μs
DISABLE Voltage-Off					0.8	V
DISABLE Voltage-On			2			V
POWER SUPPLY						
Operating Voltage Range			2.1		5.5	V
Power Supply Rejection Ratio	PSRR	V _S = +2.5V to +5.5V, V _{CM} = (-V _S) + 0.5V	74	91		dB
Quiescent Current / Amplifier	I _Q	I _{OUT} = 0		1.1	1.5	mA
DYNAMIC PERFORMANCE						
Gain-Bandwidth Product	GBP	R _L = 10kΩ, C _L = 100pF		11		MHz
Phase Margin	φ _O	R _L = 10kΩ, C _L = 100pF		51		Degrees
Full Power Bandwidth	BWP	< 1% distortion, R _L = 600Ω		400		kHz
Slew Rate	SR	G = +1, 2V Step, R _L = 10kΩ		9		V/μs
Settling Time to 0.1%	t _S	G = +1, 2V Step, R _L = 600Ω		0.3		μs
Overload Recovery Time		V _{IN} · Gain = V _S , R _L = 600Ω		1.5		μs
NOISE PERFORMANCE						
Voltage Noise Density	e _n	f = 1kHz		11.5		nV/√Hz
		f = 10kHz		8		nV/√Hz

2 Typical Performance Characteristics





3 Application Note

3.1 Size

SNA872X series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the SNA872X series packages save space on printed circuit boards and enable the design of smaller electronic products.

3.2 Power Supply Bypassing and Board Layout

SNA872X series operates from a single 2.1V to 5.5V supply or dual $\pm 1.05\text{V}$ to $\pm 2.75\text{V}$ supplies. For best performance, a $0.1\mu\text{F}$ ceramic capacitor should be placed close to the VDD pin in single supply operation. For dual supply operation, both V_{DD} and V_{SS} supplies should be bypassed to ground with separate $0.1\mu\text{F}$ ceramic capacitors.

3.3 Low Supply Current

The low supply current (typical 1.1mA per channel) of SNA872X series will help to maximize battery life. They are ideal for battery powered systems.

3.4 Operating Voltage

SNA872X series operate under wide input supply voltage (2.1V to 5.5V). In addition, all temperature specifications apply from -40°C to $+125^{\circ}\text{C}$. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime.

3.5 Rail-to-Rail Input

The input common-mode range of SNA872X series extends 100mV beyond the supply rails ($V_{\text{SS}}-0.1\text{V}$ to $V_{\text{DD}}+0.1\text{V}$). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

3.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of SNA872X series can typically swing to less than 2mV from supply rail in light resistive loads ($>100\text{k}\Omega$), and 15mV of supply rail in moderate resistive loads ($10\text{k}\Omega$).

3.7 Capacitive Load Tolerance

The SNA872X family is optimized for bandwidth and speed, not for driving capacitive loads. Output capacitance will create a pole in the amplifier's feedback path, leading to excessive peaking and potential oscillation. If dealing with load capacitance is a requirement of the application, the two strategies to consider are (1) using a small resistor in series with the amplifier's output and the load capacitance and (2) reducing the bandwidth of the amplifier's feedback loop by increasing the overall noise gain. Figure 4-1 shows a unity gain follower using the series resistor strategy. The resistor isolates the output from the capacitance and more importantly, creates a zero in the feedback path that compensates for the pole created by the output capacitance.

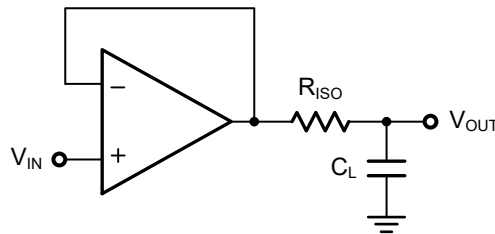


Figure 3-1 Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. However, if there is a resistive load R_L in parallel with the capacitive load, a voltage divider (proportional to R_{ISO}/R_L) is formed, this will result in a gain error.

The circuit in Figure 4-2 is an improvement to the one in Figure 4-1. R_F provides the DC accuracy by feed-forward the V_{IN} to R_L . C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased by increasing the value of C_F . This in turn will slow down the pulse response.

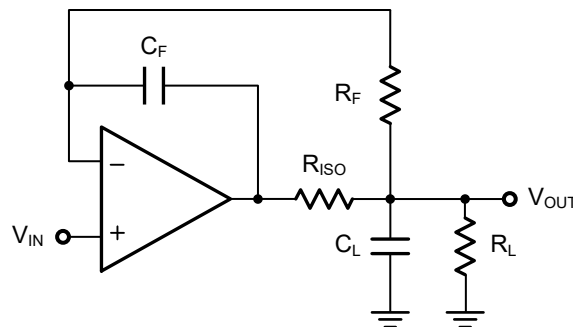


Figure 3-2 Indirectly Driving a Capacitive Load with DC Accuracy

4 Typical Application Circuits

4.1 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common to the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. Figure 5-1 shows the differential amplifier using SNA872X.

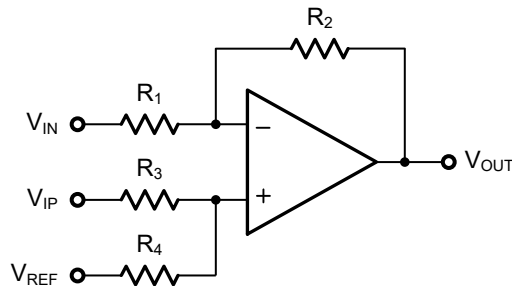


Figure 4-1 Differential Amplifier

$$V_{OUT} = \frac{(R_1 + R_2)}{(R_3 + R_4)} \frac{R_4}{R_1} V_{IN} - \frac{R_2}{R_1} V_{IP} + \frac{(R_1 + R_2)}{(R_3 + R_4)} \frac{R_3}{R_1} V_{REF}$$

If the resistor ratios are equal (i.e. $R_1=R_3$ and $R_2=R_4$), then

$$V_{OUT} = \frac{R_2}{R_1} (V_{IP} - V_{IN}) + V_{REF}$$

4.2 Low Pass Active Filter

The low pass active filter is shown in Figure 5-2. The DC gain is defined by $-R_2/R_1$. The filter has a -20dB/decade roll-off after its corner frequency $f_c = 1/(2\pi R_3 C_1)$.

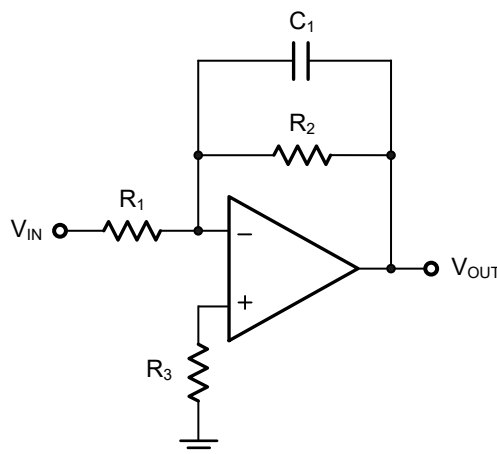


Figure 4-2 Low Pass Active Filter

4.3 Instrumentation Amplifier

The triple SNA872X can be used to build a three-op-amp instrumentation amplifier as shown in Figure 5-3. The amplifier in Figure 5-3 is a high input impedance differential amplifier with gain of R_2/R_1 . The two differential voltage followers assure the high input impedance of the amplifier.

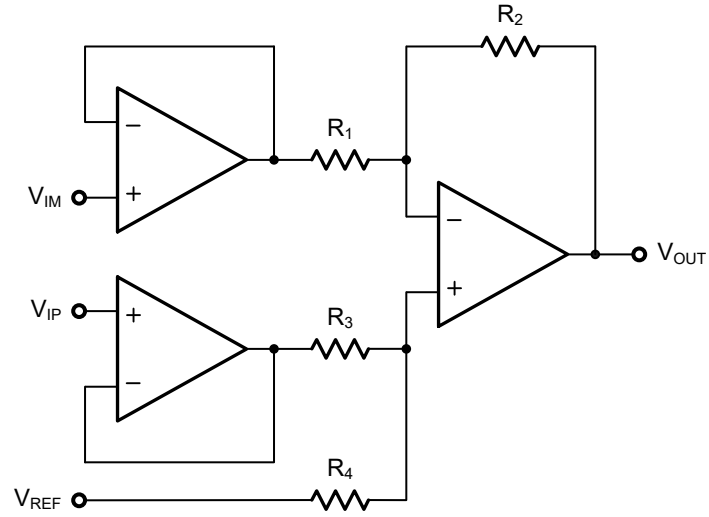
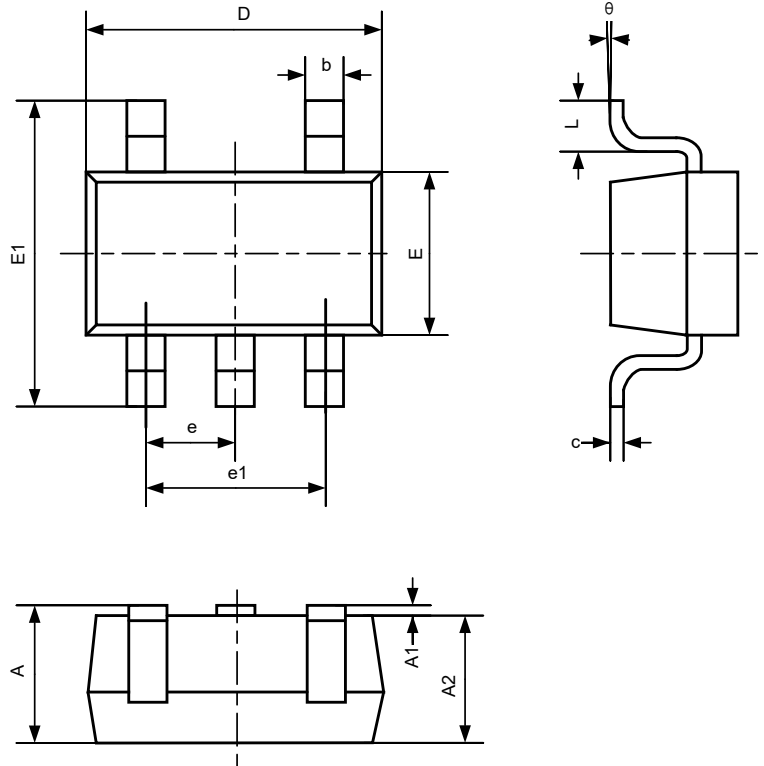


Figure 4-3 Instrument Amplifier

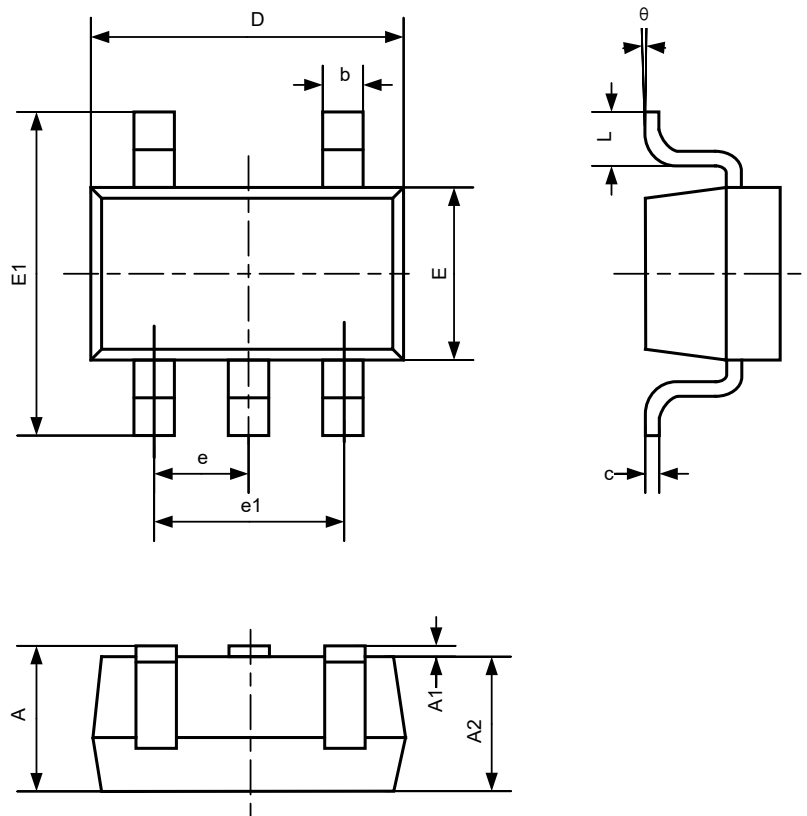
5 Package Information

5.1 SC70-5



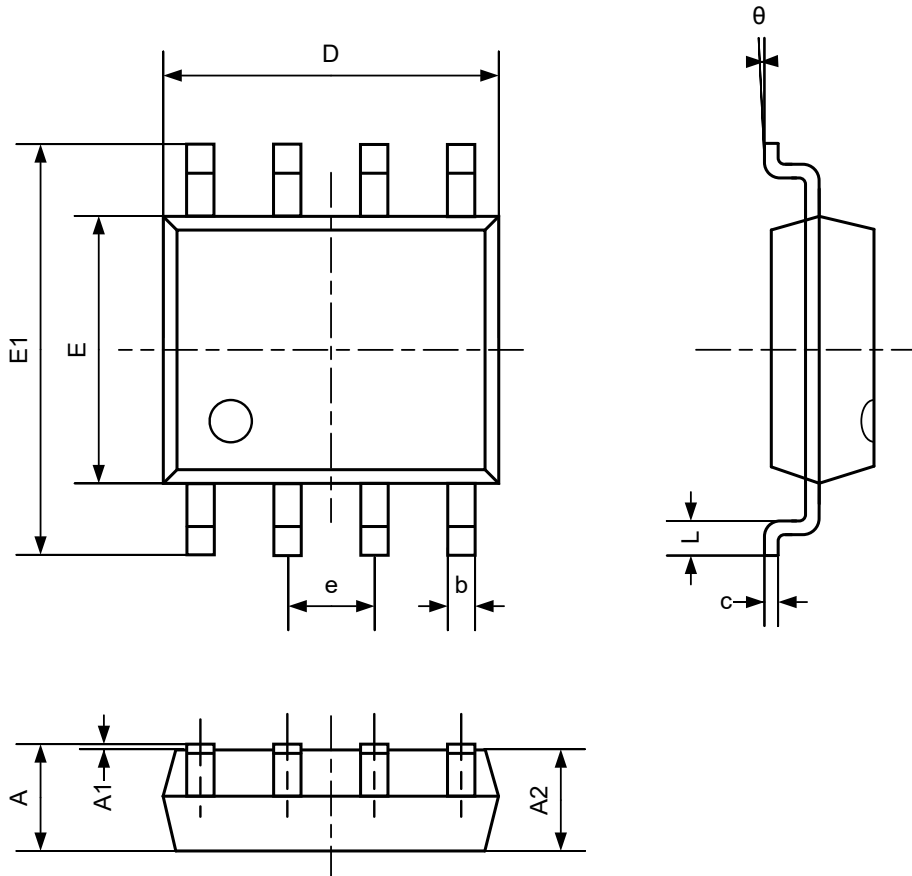
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 BSC		0.026 BSC	
e1	1.300 BSC		0.051 BSC	
L	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

5.2 SOT-23-5



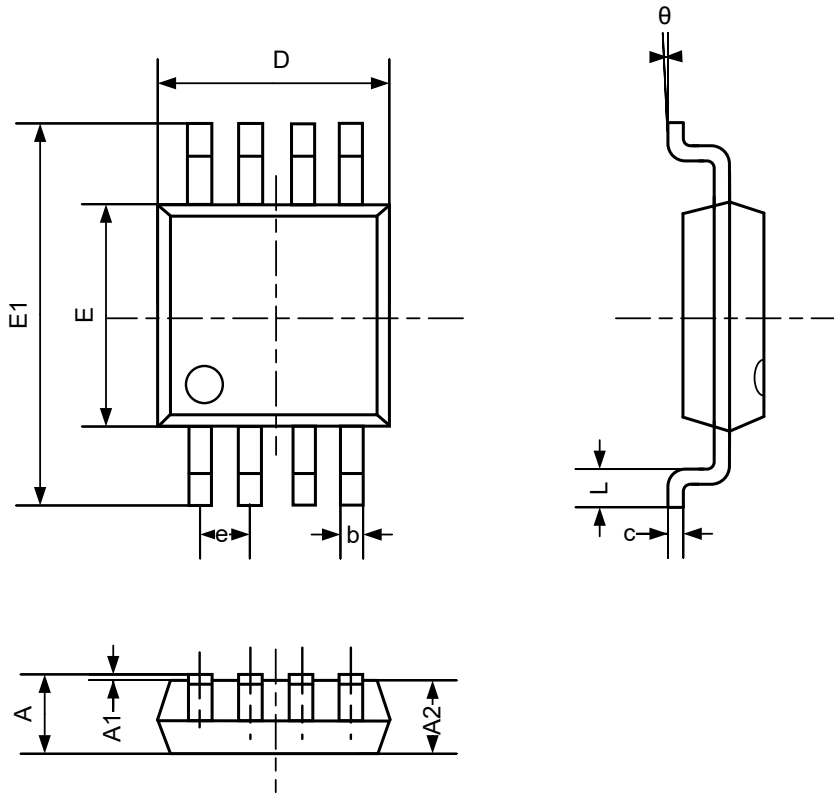
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

5.3 SOP-8



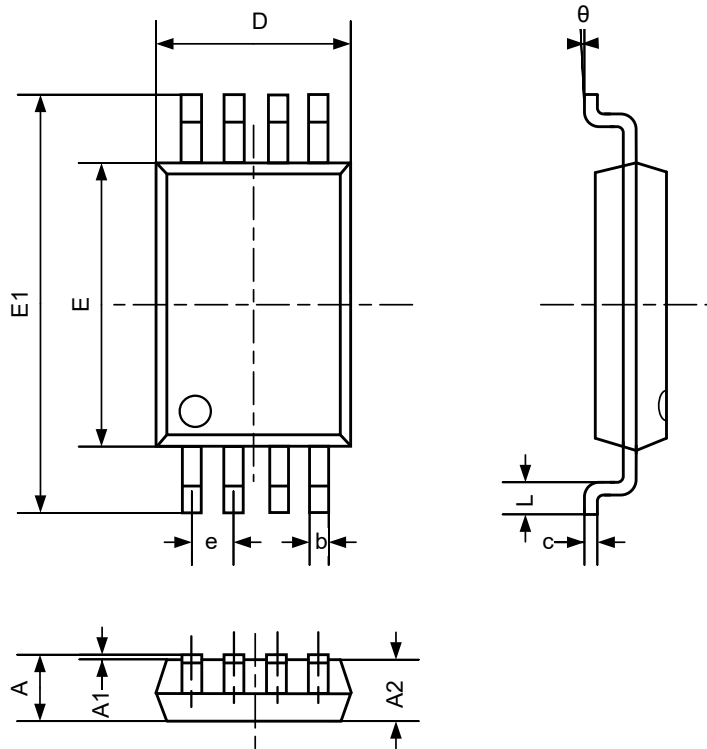
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

5.4 MSOP-8



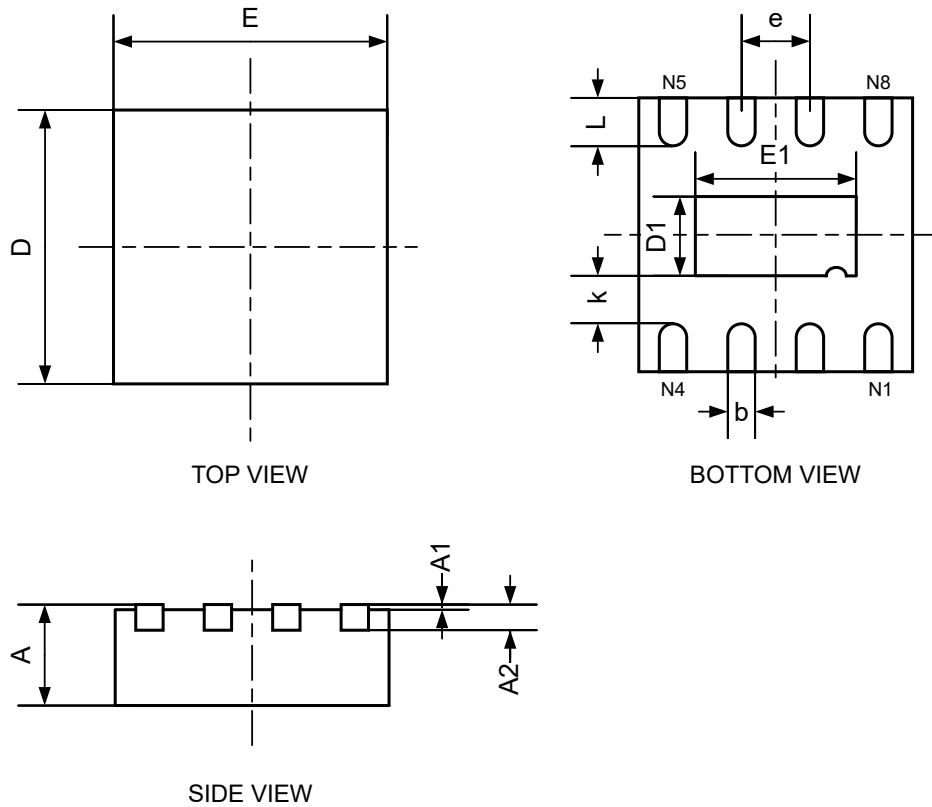
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

5.5 TSSOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	2.900	3.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

5.6 DFN2*2-8




Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.800	0.850	0.900	0.031	0.033	0.035
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	0.153	0.203	0.253	0.006	0.008	0.010
b	0.180	0.240	0.300	0.007	0.009	0.012
D	1.900	2.000	2.100	0.075	0.079	0.083
E	1.900	2.000	2.100	0.075	0.079	0.083
D1	0.500	0.600	0.700	0.020	0.024	0.028
E1	1.100	1.200	1.300	0.043	0.047	0.051
e		0.500			0.020	
k	0.200			0.008		
L	0.250	0.350	0.450	0.010	0.014	0.018

6 Revision History

Version	Date	Description
0.1	2021/10/21	Initial release
0.2	2022/07/12	Update some specification informations;;Add DFN-8 package

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